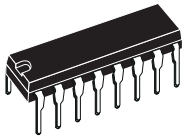
HCF4510B

PRESETTABLE BCD UP/DOWN COUNTER

- MEDIUM SPEED OPERATION : 8 MHz (Typ.) at 10V
- SYNCHRONOUS INTERNAL CARRY PROPAGATION
- RESET AND PRESET CAPABILITY
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIF. UP TO 20V
- 5V, 10V AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT I_I = 100nA (MAX) AT V_{DD} = 18V T_A = 25°C
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"



DIP

ORDER CODES

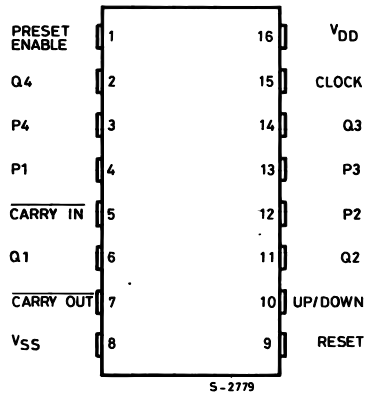
PACKAGE	TUBE	T & R
DIP	HCF4510BEY	

DESCRIPTION

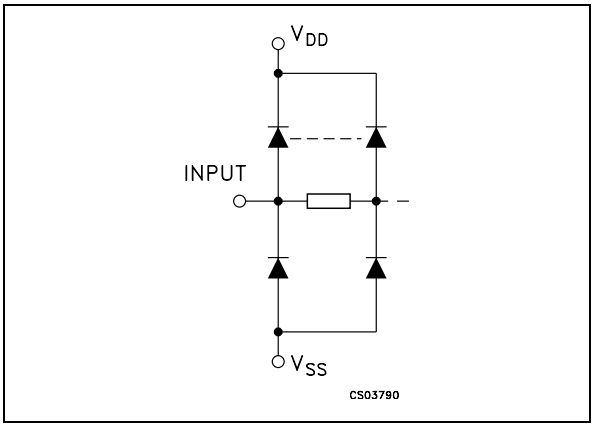
HCF4510B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP package.

It is a PRESETTABLE BCD UP/DOWN COUNTER consists of four synchronously clocked D-type flip-flops (with a gating structure to provide T-type flip-flop capability) connected as a counter. This counter can be cleared by a high level on the RESET line, and can be preset to any binary number present on the jam inputs by a high level on the PRESET ENABLE line. This device will count out of non-BCD counter states in a maximum of two clock pulses in the up mode and a maximum of four clock pulses in the down mode. If the CARRY IN input is held low, the counter advances up or down on each positive going clock transition. Synchronous cascading is accomplished by connecting all clock inputs in parallel and connecting the CARRY OUT of a less significant stage to the CARRY IN of a more significant stage. HCF4510B can be cascaded in the ripple mode by connecting all clock inputs in parallel and connecting the CARRY OUT to the clock of the next stage. If the UP/DOWN input changes during a terminal count, the CARRY OUT must be gated with the clock, and the UP/DOWN input must change while the clock is high. This method provides a clean clock signal to the subsequent counting stage.

PIN CONNECTION



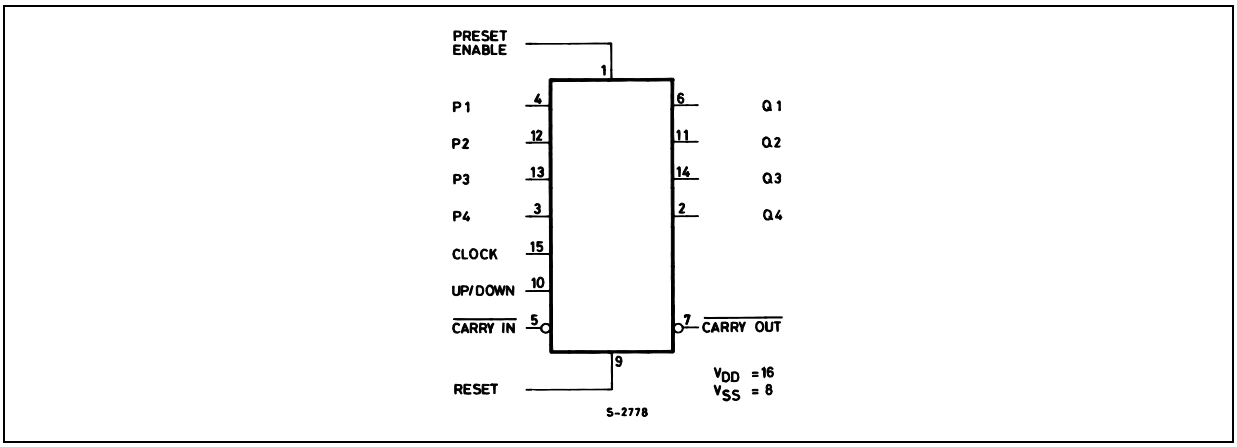
IINPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	PRESET ENABLE	Preset Enable Input
4, 12, 13, 3	P1 to P4	Inputs
6, 11, 14, 2	Q1 to Q4	Outputs
15	CLOCK	Clock Input
10	UP/DOWN	Up/Down Control Input
5	$\overline{\text{CARRY-IN}}$	Carry Input
7	$\overline{\text{CARRY-OUT}}$	Carry Output
9	RESET	Reset Input
8	V_{SS}	Negative Supply Voltage
16	V_{DD}	Positive Supply Voltage

FUNCTIONAL DIAGRAM

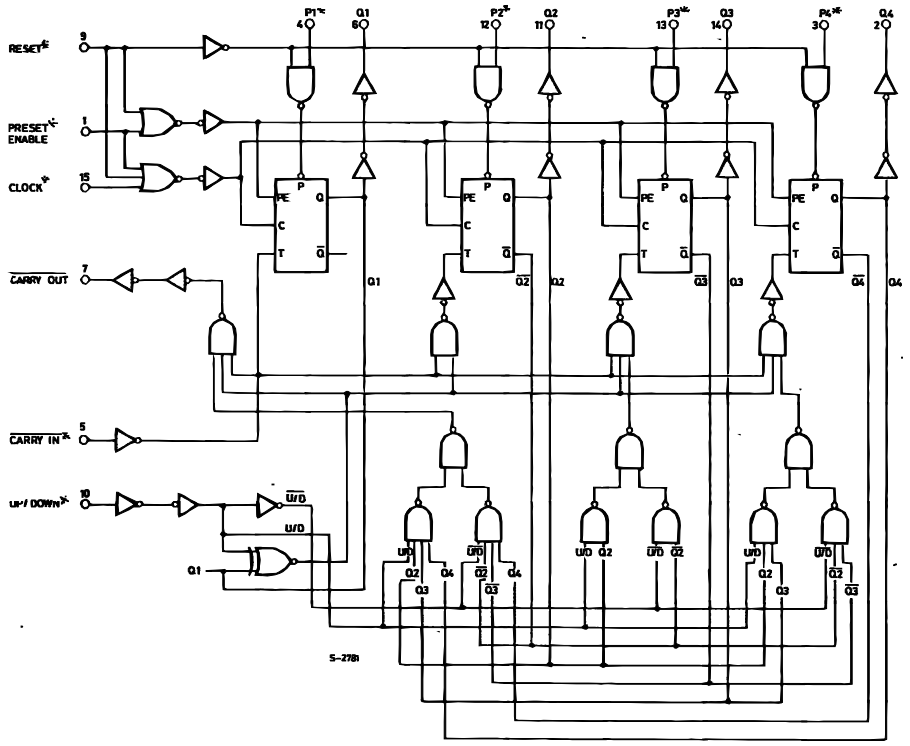


TRUTH TABLE

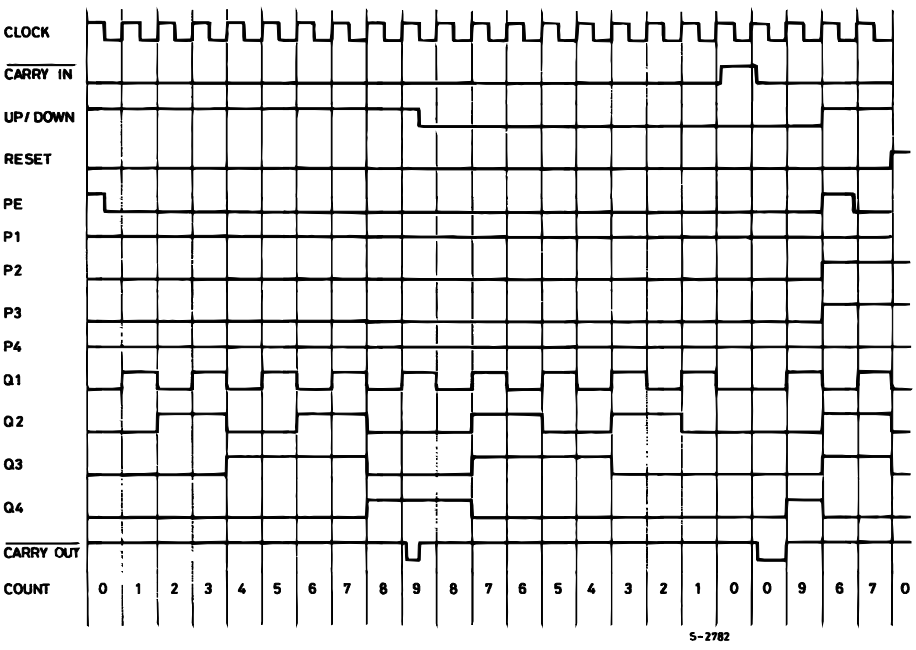
CL	$\overline{\text{CARRY-IN}}$ $\overline{\text{(CI)}}$	UP/DOWN	PRESET ENABLE	RESET	ACTION
X	H	X	L	L	NO COUNT
⎍	L	H	L	L	COUNT UP
⎍	L	L	L	L	COUNT DOWN
X	X	X	H	L	PRESET
X	X	X	X	H	RESET

X : Don't Care

LOGIC DIAGRAM



TIMING CHART



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.5 to +22	V
V_I	DC Input Voltage	-0.5 to V_{DD} + 0.5	V
I_I	DC Input Current	± 10	mA
P_D	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
T_{op}	Operating Temperature	-55 to +125	°C
T_{stg}	Storage Temperature	-65 to +150	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

All voltage values are referred to V_{SS} pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	3 to 20	V
V_I	Input Voltage	0 to V_{DD}	V
T_{op}	Operating Temperature	-55 to 125	°C

DC SPECIFICATIONS

Symbol	Parameter	Test Condition				Value							Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_A = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.	Max.	
I_L	Quiescent Current	0/5			5		0.04	5		150		150	μA
		0/10			10		0.04	10		300		300	
		0/15			15		0.04	20		600		600	
		0/20			20		0.08	100		3000		3000	
V_{OH}	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V_{OL}	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V_{IH}	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V_{IL}	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I_{OH}	Output Drive Current	0/5	2.5	<1	5	-1.36	-3.2		-1.1		-1.1		mA
		0/5	4.6	<1	5	-0.44	-1		-0.36		-0.36		
		0/10	9.5	<1	10	-1.1	-2.6		-0.9		-0.9		
		0/15	13.5	<1	15	-3.0	-6.8		-2.4		-2.4		
I_{OL}	Output Sink Current	0/5	0.4	<1	5	0.44	1		0.36		0.36		mA
		0/10	0.5	<1	10	1.1	2.6		0.9		0.9		
		0/15	1.5	<1	15	3.0	6.8		2.4		2.4		
I_I	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	±0.1		±1		±1	μA
C_I	Input Capacitance		Any Input				5	7.5					pF

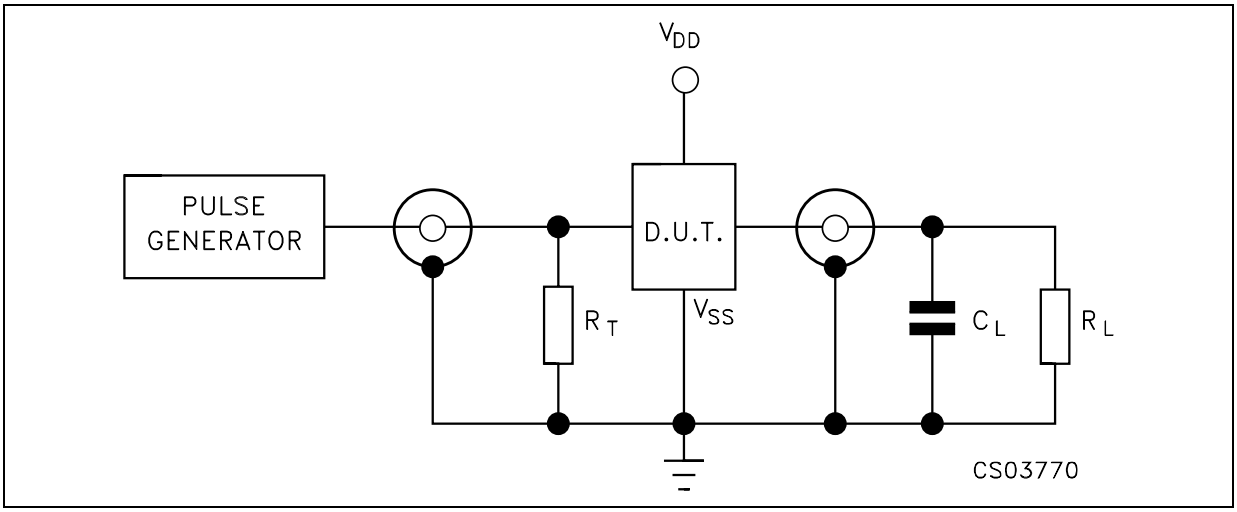
The Noise Margin for both "1" and "0" level is: 1V min. with V_{DD}=5V, 2V min. with V_{DD}=10V, 2.5V min. with V_{DD}=15V

DYNAMIC ELECTRICAL CHARACTERISTICS (T_{amb} = 25°C, C_L = 50pF, R_L = 200KΩ, $t_r = t_f$ = 20 ns)

Symbol	Parameter	Test Condition		Value (*)			Unit
		V_{DD} (V)		Min.	Typ.	Max.	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Q Output	5			200	400	ns
		10			100	200	
		15			75	150	
t_{PHL} t_{PLH}	Propagation Delay Time Preset or Reset to Q Output	5			210	420	ns
		10			105	210	
		15			80	160	
t_{PHL} t_{PLH}	Propagation Delay Time Clock to Carry Out	5			240	480	ns
		10			120	240	
		15			90	180	
t_{PHL} t_{PLH}	Propagation Delay Time Carry in to Carry Out	5			125	250	ns
		10			60	120	
		15			50	100	
t_{PHL} t_{PLH}	Propagation Delay Time Preset or Reset to Carry Out	5			320	640	ns
		10			160	320	
		15			125	250	
t_{THL} t_{TLH}	Transition Time	5			100	200	ns
		10			50	100	
		15			40	80	
f_{MAX}	Maximum Clock Frequency	5		2	4		MHz
		10		4	8		
		15		5.5	11		
t_W	Clock Pulse Width	5		150			ns
		10		75			
		15		60			
t_{REM} (1)	Preset Enable or Reset Removal Time	5		150			ns
		10		80			
		15		60			
t_r , t_f (2)	Clock Rise or Fall Time	5				15	µs
		10				5	
		15				5	
t_{setup}	Carry in Setup Time	5		130			ns
		10		60			
		15		45			
t_{setup}	Up/Down Setup Time	5		360			ns
		10		160			
		15		110			
t_W	Preset Enable or Reset Pulse Width	5		220			ns
		10		100			
		15		75			

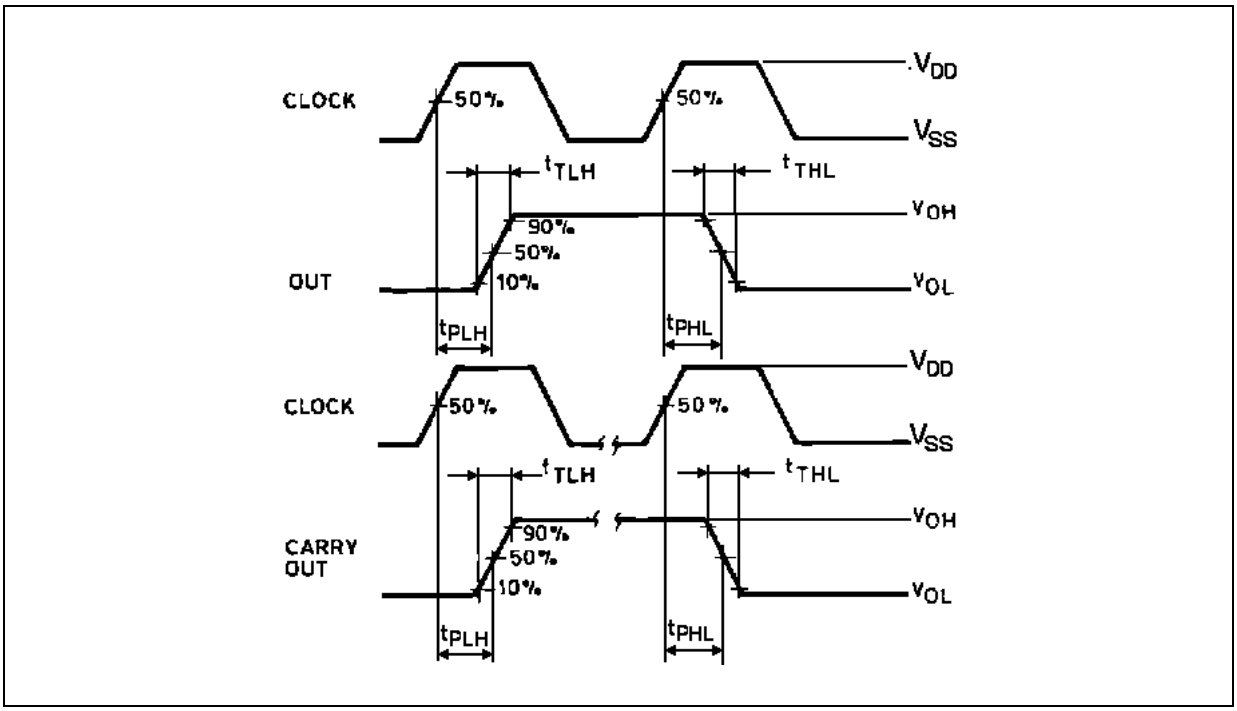
(*) Typical temperature coefficient for all V_{DD} value is 0.3 %/°C.
(1) Time required after the falling edge of the reset or preset enable inputs before the rising edge of the clock will trigger the counter (similar to setup time)
(2) If more than unit is cascaded in the parallel clocked application, trCL should be made less than or equal to the sum of the fixed propagation delay at 15pF and the transition time of the carry output driving stage for the estimated capacitive load.

TEST CIRCUIT

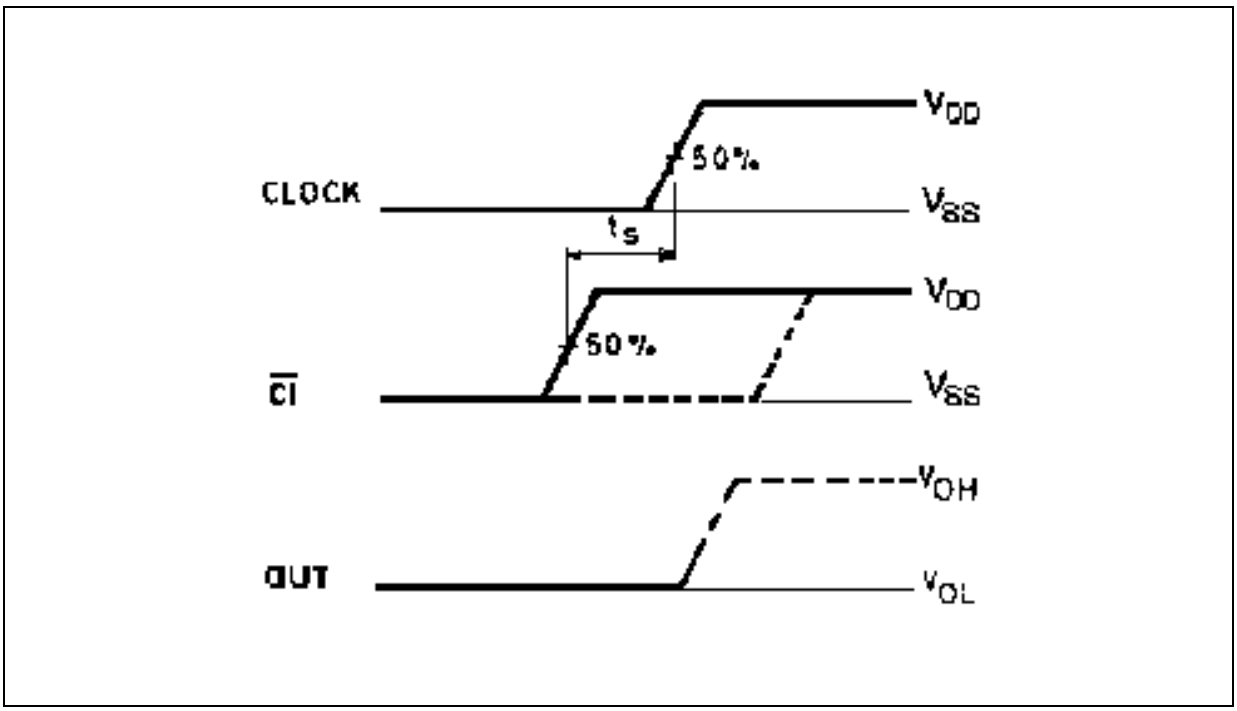


C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = 200KΩ
R_T = Z_{OUT} of pulse generator (typically 50Ω)

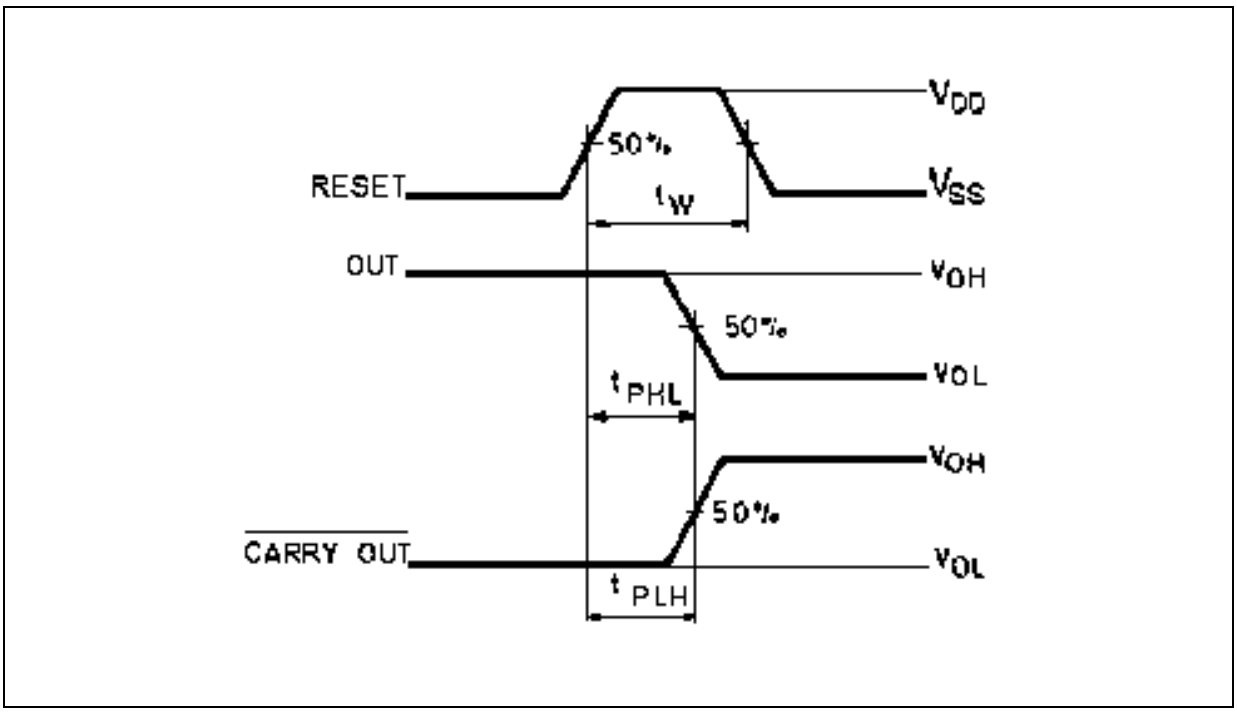
WAVEFORM 1 : PROPAGATION DELAY TIMES (f=1MHz; 50% duty cycle)



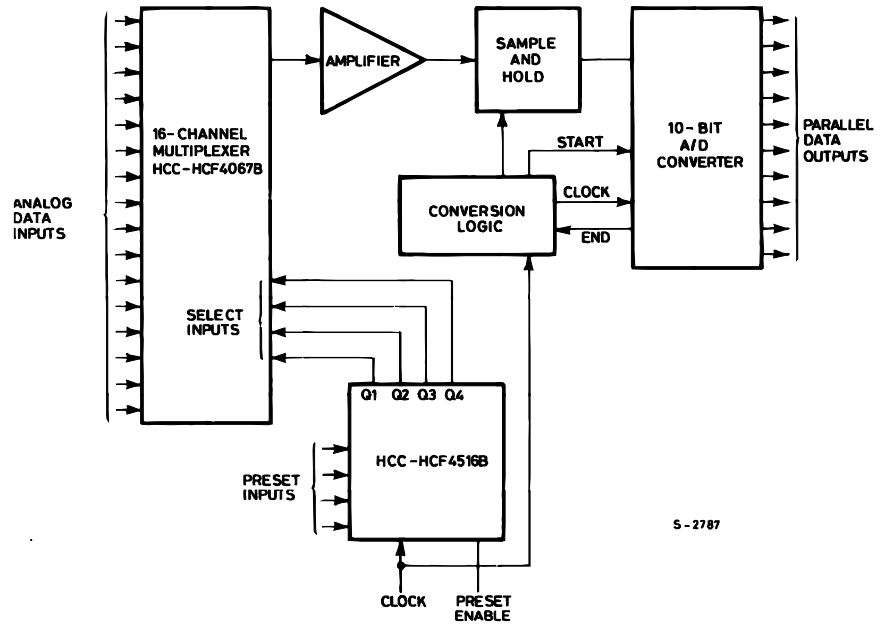
WAVEFORM 2 : MINIMUM SETUP TIME ($\overline{CI}$ TO CLOCK) (f=1MHz; 50% duty cycle)



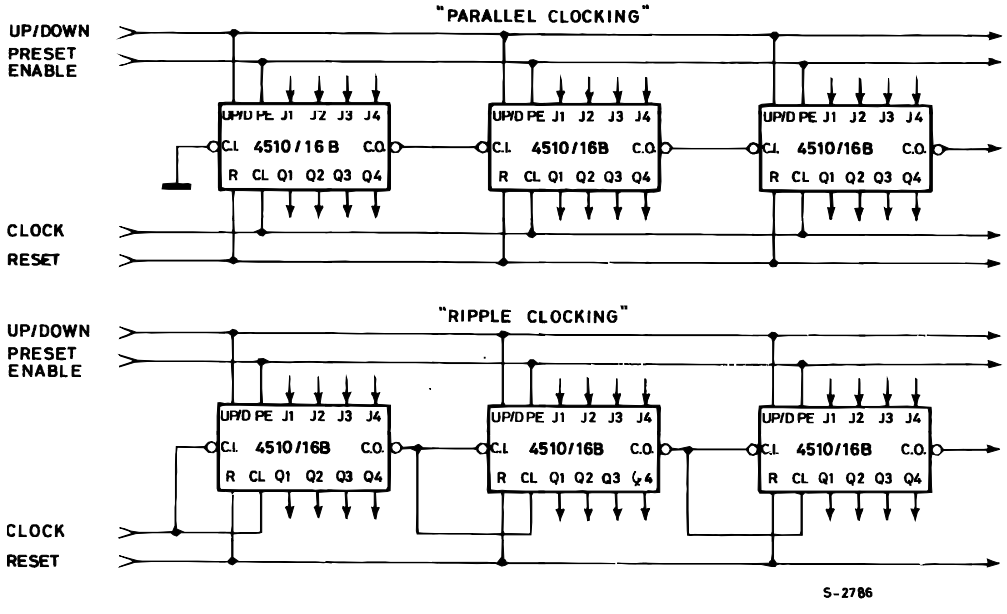
WAVEFORM 3 : PROPAGATION DELAY TIMES, MINIMUM RESET PULSE WIDTH (f=1MHz; 50% duty cycle)



TIPICAL APPLICATIONS TYPICAL 16-CHANNEL, 10 BIT DATA ACQUISITION SYSTEM

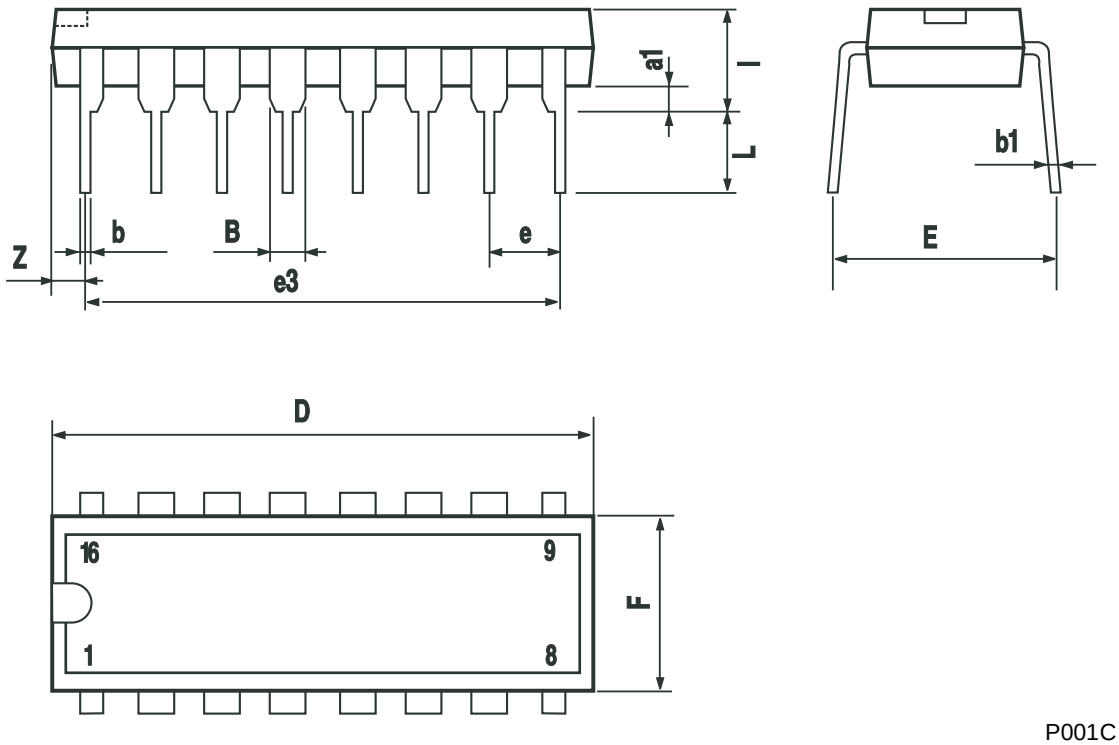


TIPICAL APPLICATIONS CASCADING COUNTER PACKAGES



Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



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